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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,238	06/19/2003	David S. Kellerman	6769-65390	5538

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EXAMINER	
DESTA, ELIAS	

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 09/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/600,238	KELLERMAN ET AL.	
	Examiner	Art Unit	
	Elias Desta	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☒ Claim(s) *11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Title

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The following title is suggested: 'A Scan Test Viewing and Analysis Tool for an Integrated Tester'

Specification

2. The specification is objected to because of the following minor informalities:

- Page 10, line 11: change the subtitle 'Data Store' to 'Data Storage'. Correction is required.

Claim Objection

3. Claims 1, 4 and 6 are objected to because of the following minor informalities:

- Claims 1, 4 and 6: change the phrase "data store" to "data storage". Correction is required.

Claim rejection – 35 U.S.C 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this

subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-10 are rejected under 35 U.S.C. 102(e) as anticipated by *Swoboda et al.* (U.S. Patent 6,704,895).

In reference to claims 1, 4, 6 and 10: *Swoboda et al.* teaches an IC tester (see *Swoboda et al.*, Fig. 23 and column 3, lines 16-20). The tester includes:

- A test head fixture (see *Swoboda et al.*, Fig. 23, member 1651, wafer head) for electrically interconnecting (member 1665) with an IC DUT (wafer 1657) to apply test signals for test program having at least one scan test and to acquire results data from execution of the test program (see *Swoboda et al.*, column 33, lines 30-65);
- A controller for causing the test head fixture to execute the test program on the IC DUT (see *Swoboda et al.*, Fig. 23, Wafer Test Head Scans in or out data through the Controller Card to the Testing Environment);
- A data Storage (see *Swoboda et al.*, Fig. 23, member 1145) having test program specification (where the system has a test program and a storage which necessarily indicates that the program resides in a storage unit such as a hard drive as shown in Fig. 23, and Fig. 31), a compiled program such as the C program (see *Swoboda et al.*, column 5, lines 33-52) and the cross reference data (see *Swoboda et al.*, column 5, lines 60-64). The archive (the data store) allows collection of group of files into a single archive which has a function of interrelating the test program specification (macros), compiled test program (EPROM programmer

format) and test execution results data (executed on a target chip) (see *Swoboda et al.*, column 6, lines 13-41); and

- A scan-test viewing tool (see *Swoboda et al.*, Fig. 24, Testing Environment Monitor) for presenting a set of views relating to the scan test on a display for viewing by the user, the views includes a cyclic view of an execution of test program that is necessarily present because simulation executing code includes single/multiple cycle counts (see *Swoboda et al.*, column 6, lines 27-41). Further the scan test-viewing tool includes the procedural view of the test program (see *Swoboda et al.*, Fig. 15), and resulting scan vector (initial state or test vector) (see *Swoboda et al.*, column 18, lines 35-42). The scan test viewing tool provides navigational links for navigating between a location in one of the views to a correlated location in another of the views is necessarily present because the system in *Swoboda et al.* Fig. 2 shows that the system has an emulation feature to emulate the wafer scale chips, or IC as shown in Fig. 23.

With regard to claims 2 and 7: as noted above in claims 1 and 6, *Swoboda et al.* further teaches that IC tester further includes a test program compiler (see *Swoboda et al.*, Fig. 1) for compiling a definition of the test program into a version of the program executable on the test, and also producing the cross reference data interrelating the test program scan sells and signals of the IC DUT (Wafer Scale IC's) (see *Swoboda et al.*, column 5, lines 58-64).

With regard to claim 3, as noted above in claim 1, *Swoboda et al.* further teaches that the controller also produces the cross reference data interrelating the test results with the test program, scan cells and signals of the IC DUT because the controller card in *Swoboda et al.*

communicates with the PC card through serial port and provides emulation of a complete solution from development through manufacture and field test (see *Swoboda et al.*, Fig. 2 and column 7, lines 31-43).

With regard to claims 5 and 9: as noted above in claims 4 and 6, *Swoboda et al.* further teaches the IC scan test includes a software programming with an editing function allowing the user to edit definition of the test program because the system in *Swoboda et al.* includes a macro modules and library modules (see *Swoboda et al.*, column 5, lines 60-64). The reverse assembly allows the user to edit and reassemble the source code or statements (see *Swoboda et al.*, column 6, lines 34-41).

With regard to claim 8: as noted above in claim 6, *Swoboda et al.* further teaches that the computer-readable program carrying medium (such as hard disc drive 1145 shown in Fig. 23) include a test execution controller for causing the tester to perform a test of the IC DUT (Wafer scale chips, 1657) according to the test program specification for receiving test execution results from the tester, and for producing a cross reference data because the assembler includes macro capabilities, library functions, conditional assembly, re-locatable modules, complete error diagnostics, symbol table and cross reference (as noted in column 5, lines 58-64) which is executed from the host computer (see *Swoboda et al.*, column 33, lines 30-39).

Allowable Subject Matter

6. *Claim 11* is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. Citation of pertinent prior art:

- *Eldridge et al.* (U.S. PAP 2004/0004216) teaches test assembly including test die for testing semiconductor product die.
- *Danialy et al.* (U.S. PAP 2002/0073374) teaches method, system and program product for testing and/or diagnosing circuits using embedded test controller access data.
- *Sato et al.* (U.S. PAP 2001/0022743) teaches semiconductor integrated circuit device and a technique for manufacturing the semiconductor integrated circuit device and more particularly to a design for testability capable of reducing an over-head caused by having a test circuit in the semiconductor integrated circuit.
- *Winters* (IEEE Article, 'Using IEEE-1149.1 For In-Circuit Emulation') teaches an over view of JTAG based emulator with a boundary-scan based debugging features.
- *Burgess Jr. et al.* (IEEE Article, 'The Boundary Scan') teaches a the problem caused by miniaturization trends in integrated circuit technology.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elias Desta whose telephone number is (571)-272-2214. The examiner can normally be reached on M-Thu (8:30-7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (571)-272-2216. The fax phone numbers for the

organization where this application or proceeding is assigned are (703)-308-5841 for regular communications and After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-308-1782.

Elias Desta
Examiner
Art Unit 2857

-ed

August 30, 2004

MARC S. HOFF
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800